

oxidizing the surface of the silicon substrate to form a gate oxide layer having a thickness greater than the first thickness.

53. (New) The process of claim 52, wherein implanting in predetermined regions is an ion implantation step.
54. (New) The process of claim 52, wherein growing a silicon oxide layer comprises oxidation in a furnace, by plasma oxidation, electrochemical oxidation or rapid thermal oxidation.
55. (New) The process of claim 52, wherein growing the silicon oxide layer comprises an oxidation step in a furnace at a temperature of at least 300°C and in an oxidizing atmosphere.

Response to Office Action Mailed July 10, 2002

A. Claims In The Case

Claims 1, 3-7, 9, 11, 12, and 14-17 have been rejected. Claims 1, 3-7, 9, 11, 12, and 14-17 have been canceled without prejudice. Claims 18-55 have been added. Claims 18-55 are pending in the case.

B. The Claims Are Not Anticipated By Bergeron Pursuant To 35 U.S.C. § 102

The Examiner rejected claims 1, 3-5, 9, 11, 12, and 14-16 as being anticipated by U.S. Patent No. 4,157,268 to Bergeron et al. (hereinafter referred to as "Bergeron"). Applicant respectfully disagrees with these rejections.

Applicant has canceled the rejected claims and added new claims 18-57. Independent claims 18, 23, 28, and 33 are directed to a process for forming a semiconductor device comprising a plurality of MOS transistors. Independent claims 37, 42, 47, and 52 are directed to a semiconductor device comprising a plurality of MOS transistors. Applicant submits that Bergeron does not appear to teach or suggest a process for the formation of a MOS transistor. Furthermore, Applicant submits that Bergeron does not appear to teach a semiconductor device comprising a plurality of MOS transistors. Reconsideration of this rejection is respectfully requested.

C. The Claims Are Not Anticipated By Wu Pursuant To 35 U.S.C. § 102

The Examiner rejected claims 1, 3-5, 9, 11, 12, and 14-16 as being anticipated by U.S. Patent No. 5,863,826 to Wu et al. (hereinafter referred to as "Wu"). Applicant respectfully disagrees with these rejections.

Applicant has canceled the rejected claims and added new claims 18-57. Independent claims 18, 23, 28, and 33 are directed to a process for forming a semiconductor device comprising a plurality of MOS transistors.

Independent claims 18, 23, 28, and 33 all recite, in part:

implanting, in the predetermined regions of the silicon substrate, a chemical species ...;
oxidizing the surface of the silicon substrate to form a gate oxide layer of non uniform thickness; and
forming MOS transistors at the predetermined regions of the silicon substrate, wherein the oxidized layer at the predetermined regions forms the gate oxide layer of the MOS transistors.

Applicant submits that the features of independent claims 18, 23, 28, and 22 do not appear to be taught or suggested by Wu.

Wu states:

Typically, a rapid thermal anneal occurs in a dry O₂ ambient at 1000 deg C. for 5 minutes. As shown in FIG. 3, enhanced oxidation occurs in the porous field isolation regions 42 because of the increased surface area of the pores 37 (FIG. 2) and the high reactivity of unsaturated silicon bonds on these surfaces. In contrast, a relatively thin layer of oxide 44 grows over the single crystal silicon in the active regions 46. At this point, the thin oxide layer 44 over the active regions 46 can, for example, function as a gate oxide or as a sacrificial oxide for a subsequent channel implant.

(Wu, col. 4, lines 24-33)

Applicant submits that Wu appears to teach the use of implantation to produce thick oxide regions on a silicon substrate that are used as isolation regions. Wu appears to teach that the oxide layers grown on the portion of the silicon substrate in which an implantation does not occur may be used to form a gate oxide. As such, Applicant submits that Wu does not appear to teach or suggest all of the features of applicant's claims. Reconsideration of this rejection is respectfully requested.

The Examiner states that "it would be obvious to one of ordinary skill in the art to use routine experimentation to find an appropriate ion dosage level because methods of doing so are well known in the art." Applicant respectfully disagrees.

Applicant submits that the relationship between the oxide thickness and the implantation conditions (dose and energy) would not be obvious to one of ordinary skill in the art. As shown in table 1, at an implanted dose of 5×10^{14} at/cm² and with an energy of 2 keV, the thickness of the oxide layer formed is 5.66 nm, while at the same

implanted dose of 5×10^{14} at/cm² and with an energy of 80 keV, the thickness of the oxide layer formed is 6.00 nm. Therefore, with a 40 times increase in energy used, the increase in thickness is minimal.

Additionally, at an implanted dose of 5×10^{16} at/cm² and with an energy of 10 keV, the thickness of the oxide layer formed is 12.3 nm, while at the same implanted dose, but at an energy of 80 keV, the thickness of the oxide layer formed is 11.0 nm. In this case the thickness decreases while energy increases. Applicant submits that the use of low energy levels between 2 and 15 keV leads, unexpectedly, to about the same thicknesses of the oxide layer formed at a region implanted with ions at an energy of 80 keV. Applicant submits that the dosage limitation recited in Applicant's claims are neither taught nor suggested by the cited references. Furthermore, Applicant submits that the dosage limitation recited in Applicant's claims would not be obvious to one of ordinary skill in the art.

Independent claims 37, 42, 47, and 52 are directed to a semiconductor device comprising a plurality of MOS transistors. For at least the same reasons cited above, Applicant submits that the features of claims 37, 42, 47, and 52 are not taught or suggested by Wu.

D. The Claims Are Not Obvious Over The Cited Art Pursuant To 35 U.S.C. § 103(a)

The Examiner has rejected claims 6 and 7 as being unpatentable over Bergeron in view of U.S. Patent No. 5,215,934 to Tzeng. Applicant submits that new claims 18-55 are patentable over the cited references for at least the same reasons recited above.

E. Summary

Based on the above, Applicant submits that all claims are now in condition for allowance.

Favorable reconsideration is respectfully requested.

Applicant respectfully requests a one month extension of time to respond to the Office Action mailed July 10, 2002. A fee authorization form in the amount of \$744.00 is enclosed to cover fees for the extension of time fee and the added claims fee. If any further extension of time is required, applicant hereby requests the appropriate extension of time. If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to Conley, Rose & Tayon, P.C. Deposit Account Number 50-1505/5310-03000/EBM

Respectfully submitted,



Mark R. DeLuca
Reg. No. 44,649

Patent Agent for Applicant

CONLEY, ROSE & TAYON, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398
(512) 703-1423 (voice)
(512) 703-1250 (facsimile)

Date: 11/8/02